

REV:1.3

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1156-A
05	CPU LGA1156-B
06	CPU LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH_FDI,DMI,USB,PCIE,NVRAM
11	PCH_DP,CLK BUFFER
12	PCH_HOST,SATA,PCI
13	PCH_GPIO,CTRL,AUDIO
14	PCH_PWR,GND
15	PCI_EXPRESS*16_SLOT
16	PCI_EXPRESS*1_SLOT
17	PCI_SLOT_1,2
18	ITE 8720 LPC IO
19	Dual BIOS,PHOT,D-OC
20	ALC888B-VD2
21	REAR AUDIO JACK
22	CLOCK_GEN RTM885N-914
23	DISCRETE POWER
24	ISL6545 DDR 15V,CPU VTT,PWR_SEQ
25	CPU_VAXG_PWM ISL6314CRZ
26	VCORE_PWM ISL6333CR
27	F_PANEL , F_USB , FDD

SHEET

TITLE

[illegible]

GA-H55M-S2

Version: 1.3

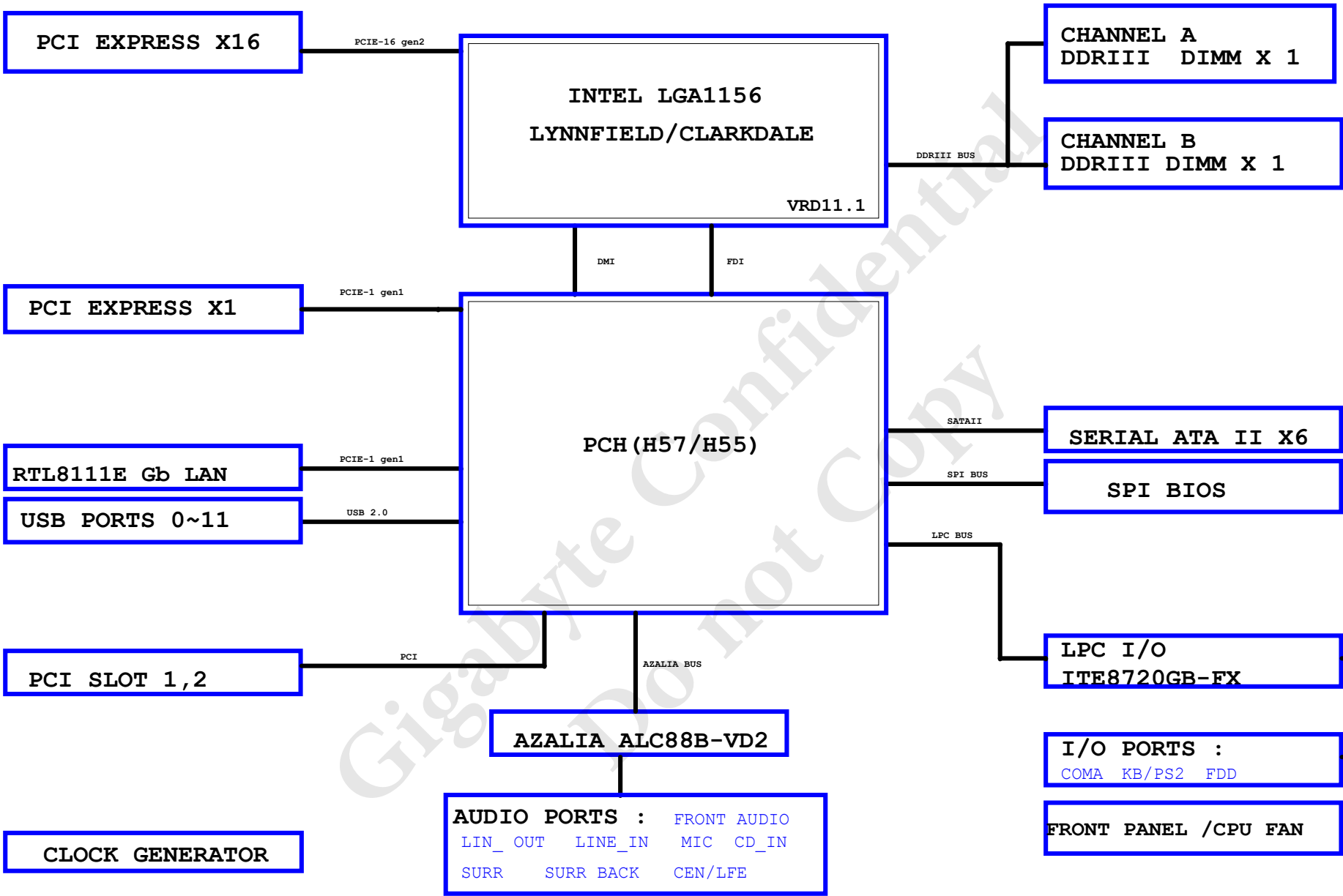
Circuit or PCB layout change
for next version

Component value change history

2010/06/03

[illegible][illegible]

BLOCK DIAGRAM



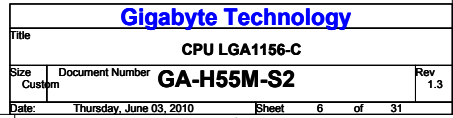
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MAAA0	AW18	SA_MA[0]	AK3 DQSA0
MAAA1	AY15	SA_MA[1]	AK3 -DQSA0
MAAA2	AW15	SA_MA[2]	AK2 DMA0
MAAA3	AU15	SA_MA[3]	
MAAA4	AW14	SA_MA[4]	AH1 MDA0
MAAA5	AY13	SA_MA[5]	AJ4 MDA1
MAAA6	AV14	SA_MA[6]	AL2 MDA2
MAAA7	AW13	SA_MA[7]	AL1 MDA3
MAAA8	AU14	SA_MA[8]	AG2 MDA4
MAAA9	AW12	SA_MA[9]	AH2 MDA5
MAAA10	AT19	SA_MA[10]	AK1 MDA6
MAAA11	AU13	SA_MA[11]	AK2 MDA7
MAAA12	AW11	SA_MA[12]	
MAAA13	AU24	SA_MA[13]	AP2 DQSA1
MAAA14	AT11	SA_MA[14]	AP3 -DQSA1
MAAA15	AR10	SA_MA[15]	AN1 DMA1
[7] -SWEA	AT22	SA_WE#	AN3 MDA8
[7] -SCASA	AU22	SA_CAS#	AN2 MDA9
[7] -SRASA	AT20	SA_RAS#	AR3 MDA10
[7] SBAA0	AV20	SA_BS[0]	AR2 MDA11
[7] SBAA1	AU19	SA_BS[1]	AM3 MDA12
[7] SBAA2	AU12	SA_BS[2]	AM2 MDA13
		SA_BS[3]	AP1 MDA14
		SA_BS[4]	AR4 MDA15
[7] -CSA0	AV21	SA_CS#	
[7] -CSA1	AW24	SA_CS#	AL4 DQSA2
	AU21	SA_CS#	AL3 -DQSA2
	AU23	SA_CS#	AL1 DMA2
[7] CKEA0	AW10	SA_CKE[0]	AT4 MDA16
[7] CKEA1	AW10	SA_CKE[1]	AU2 MDA17
	AV10	SA_CKE[2]	AW3 MDA18
	AY10	SA_CKE[3]	AW4 MDA19
		SA_CKE[4]	AT3 MDA20
MODT_A0	AV23	SA_ODT[0]	SA_ODT[0]
MODT_A1	AV24	SA_ODT[1]	SA_ODT[1]
	AW23	SA_ODT[2]	SA_ODT[2]
	AY24	SA_ODT[3]	SA_ODT[3]
[7] DCLKA0	AR22	SA_CK[0]	AY6 DQSA3
[7] -DCLKA0	AR21	SA_CK#	AW6 -DQSA3
[7] DCLKA1	AP18	SA_CK#	AW6 DMA3
[7] -DCLKA1	AN18	SA_CK[1]	
	AN21	SA_CK#	AW5 MDA24
	AP21	SA_CK#	AY5 MDA25
	AP19	SA_CK#	AU8 MDA26
	AN19	SA_CK#	AY8 MDA27
		SA_CK#	AU5 MDA28
		SA_CK#	AV6 MDA29
		SA_CK#	AV7 MDA30
		SA_CK#	AW7 MDA31
[7.8] -DDR3_RST	AV8	SM_DRAMRST#	
	AK22	SA_CS#	AR28 DQSA4
	AM22	SA_CS#	AT29 -DQSA4
	AL23	SA_CS#	AN29 DMA4
	AK23	SA_CS#	
		SA_CS#	AN27 MDA32
	AL10	SA_CS#	AT28 MDA33
	AM10	SA_CS#	AP28 MDA34
	AP10	SA_CS#	AP30 MDA35
	AN10	SA_CS#	AP27 MDA36
	AR11	SA_CS#	AP27 MDA37
	AP11	SA_CS#	AR29 MDA38
	AK9	SA_CS#	AN30 MDA39
	AK11	SA_CS#	
	AM11	SA_CS#	AV32 DQSA5
		SA_CS#	AW32 -DQSA5
		SA_CS#	AW31 DMA5
		SA_CS#	
		SA_CS#	AU30 MDA40
		SA_CS#	AU31 MDA41
		SA_CS#	AV33 MDA42
		SA_CS#	AU34 MDA43
		SA_CS#	AV30 MDA44
		SA_CS#	AW30 MDA45
		SA_CS#	AU33 MDA46
		SA_CS#	AW33 MDA47
		SA_CS#	
		SA_CS#	AW36 DQSA6
		SA_CS#	AV35 -DQSA6
		SA_CS#	AU35 DMA6
		SA_CS#	
		SA_CS#	AW35 MDA48
		SA_CS#	AY35 MDA49
		SA_CS#	AV37 MDA50
		SA_CS#	AU37 MDA51
		SA_CS#	AY34 MDA52
		SA_CS#	AW34 MDA53
		SA_CS#	AV36 MDA54
		SA_CS#	AW37 MDA55
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		SA_CS#	AR30 DQSA7
		SA_CS#	AR38 -DQSA7
		SA_CS#	AT38 DMA7
		SA_CS#	
		SA_CS#	AT39 MDA56
		SA_CS#	AT40 MDA57
		SA_CS#	AN38 MDA58
		SA_CS#	AN39 MDA59
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		SA_CS#	AP39 MDA61
		SA_CS#	AP40 MDA62
		SA_CS#	AP40 MDA63

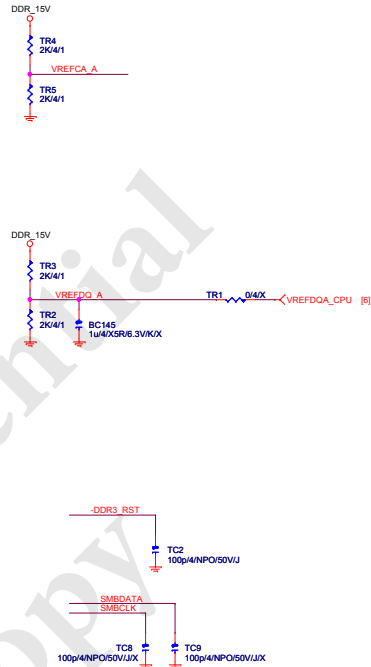
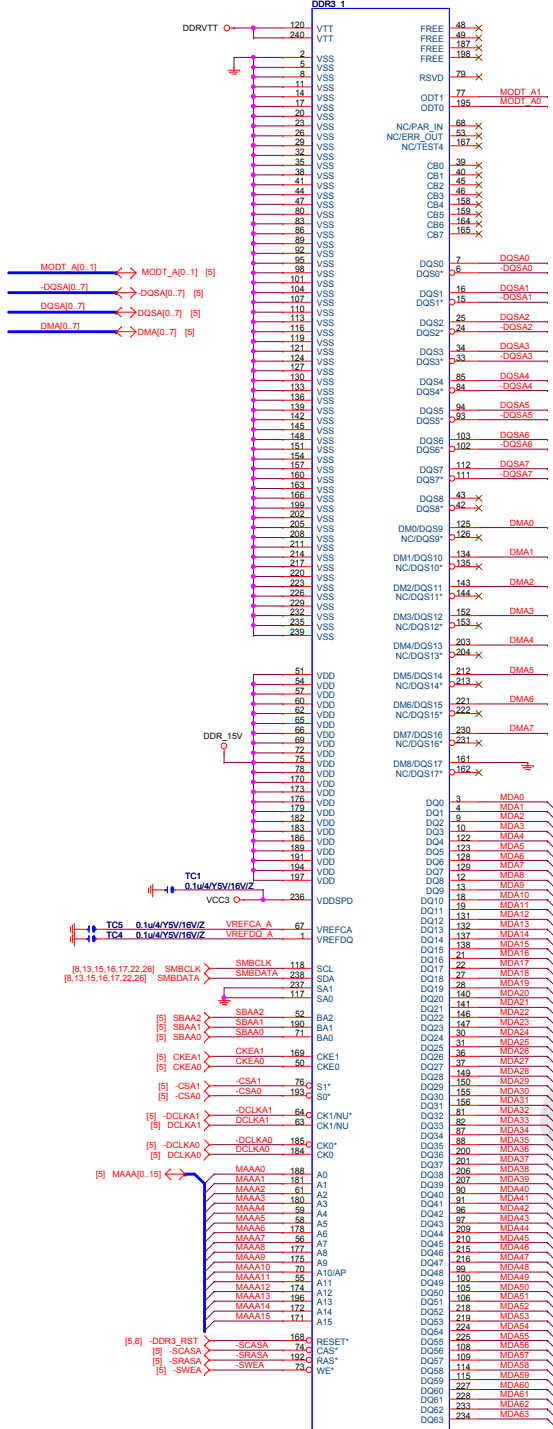
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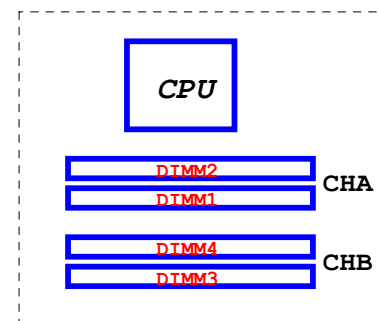
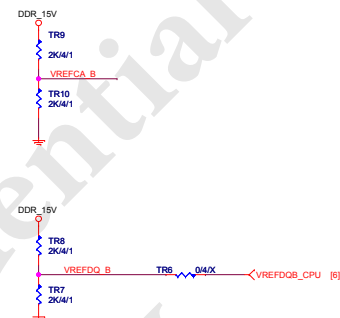
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LGA1156(10SC1-F01156-04R)

LGA1156B			
MAAB0	AU20	SB_MA[0]	AF4 DQSB0
MAAB1	AU18	SB_MA[1]	AE5 -DQSB0
MAAB2	AV18	SB_MA[2]	AE4 DMB0
MAAB3	AU17	SB_MA[3]	
MAAB4	AY18	SB_MA[4]	AD7 MDB0
MAAB5	AV17	SB_MA[5]	AD6 MDB1
MAAB6	AW17	SB_MA[6]	AH8 MDB2
MAAB7	AU16	SB_MA[7]	AJ8 MDB3
MAAB8	AT17	SB_MA[8]	AC7 MDB4
MAAB9	AY16	SB_MA[9]	AC6 MDB5
MAAB10	AY25	SB_MA[10]	AF5 MDB6
MAAB11	AW16	SB_MA[11]	AE6 MDB7
MAAB12	AY28	SB_MA[12]	
MAAB13	AW15	SB_MA[13]	AH6 DQSB1
MAAB14	AY12	SB_MA[14]	AJ5 -DQSB1
MAAB15	AV11	SB_MA[15]	AH4 DMB1
[8] -SWEB	AW26	SB_WE#	AG5 MDB8
[8] -SCASB	AW27	SB_CAS#	AH7 MDB9
[8] -SRASB	AW26	SB_RAS#	AK6 MDB10
[8] SBAB0	AW25	SB_BS[0]	AL4 MDB11
[8] SBAB1	AW25	SB_BS[1]	AC6 MDB12
[8] SBAB2	AW12	SB_BS[2]	AC4 MDB13
		SB_BS[3]	AJ7 MDB14
		SB_BS[4]	AK7 MDB15
[8] -CSB0	AY27	SB_CS#	
[8] -CSB1	AW28	SB_CS#	AN6 DQSB2
	AW28	SB_CS#	AM6 -DQSB2
	AW28	SB_CS#	AM7 DMB2
	AW28	SB_CS#	
[8] CKEB0	AW8	SB_CKE[0]	AL6 MDB16
[8] CKEB1	AW9	SB_CKE[1]	AN6 MDB17
	AW9	SB_CKE[2]	AP6 MDB18
	AW9	SB_CKE[3]	AR5 MDB19
MODT_B0	AU27	SB_ODT[0]	AL5 MDB20
MODT_B1	AU29	SB_ODT[1]	AM4 MDB21
	AV27	SB_ODT[2]	AN7 MDB22
	AV28	SB_ODT[3]	AP5 MDB23
	AV28	SB_ODT[4]	
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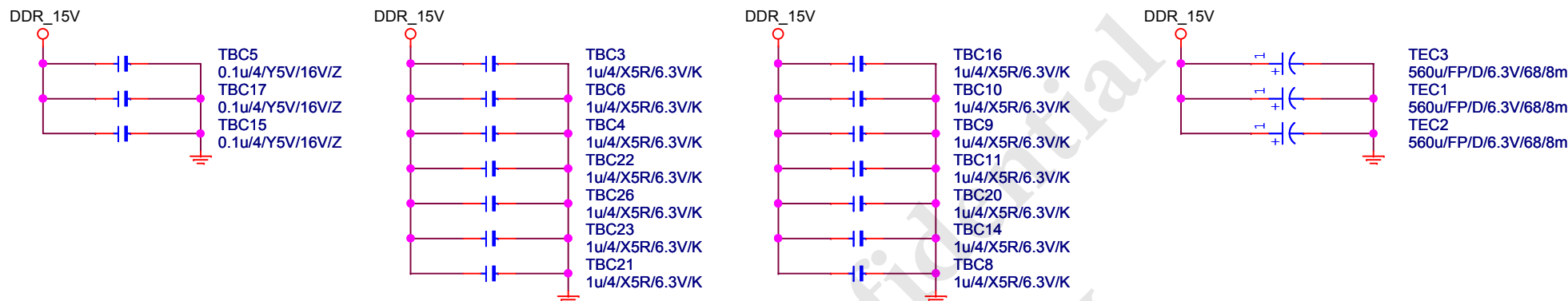




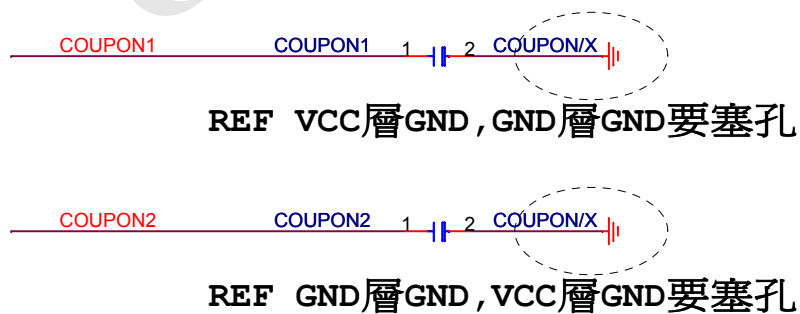
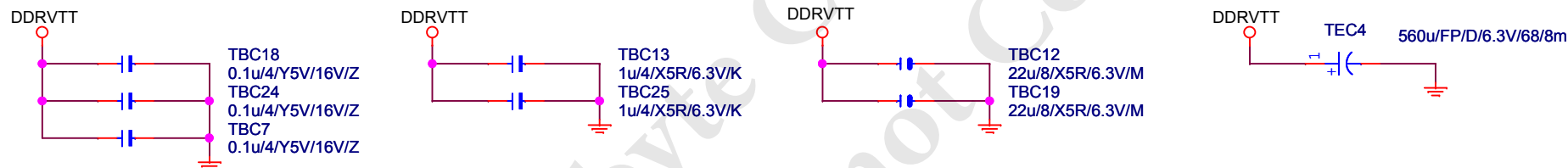


DDR TERMINATION CHANNEL A/B

DDR15V Decouple



DDRVTT Decouple

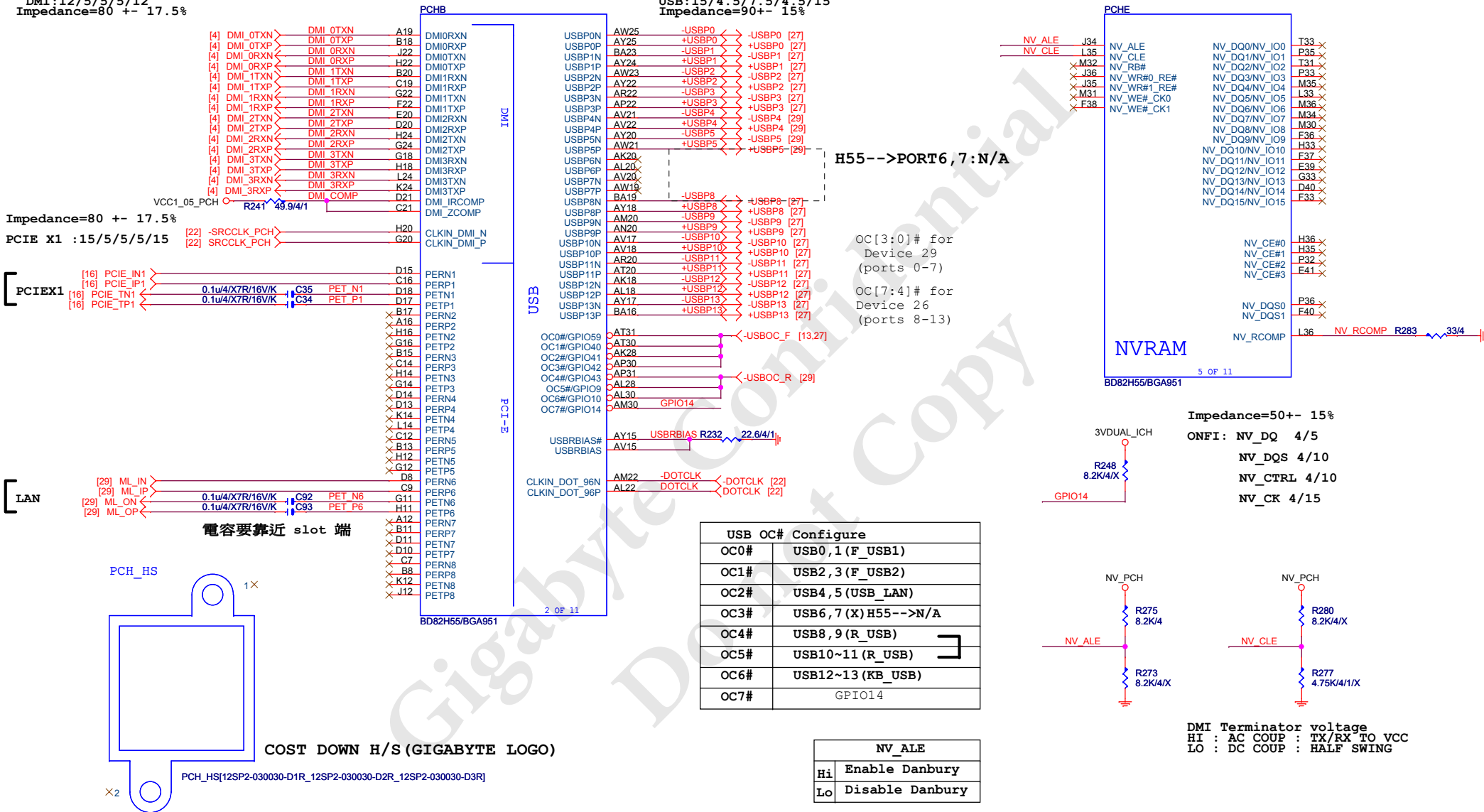


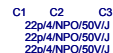
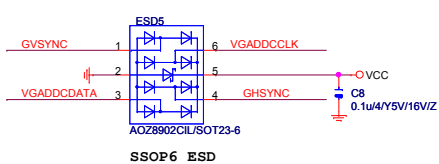
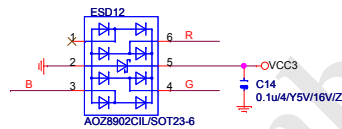
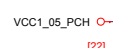
Gigabyte Technology

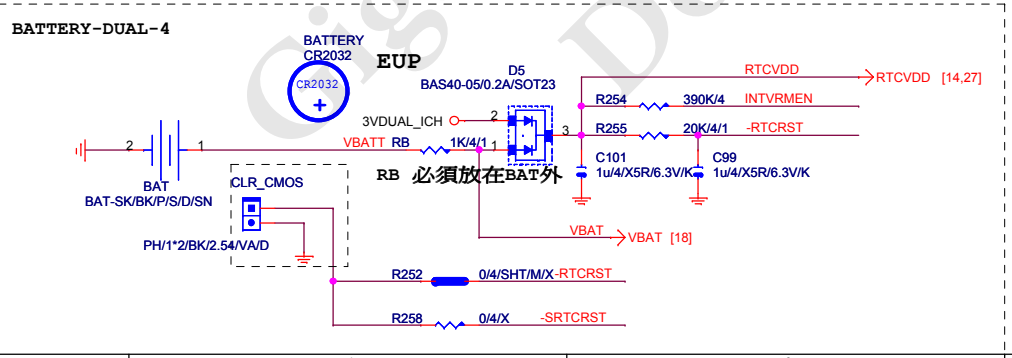
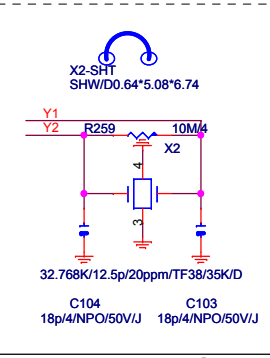
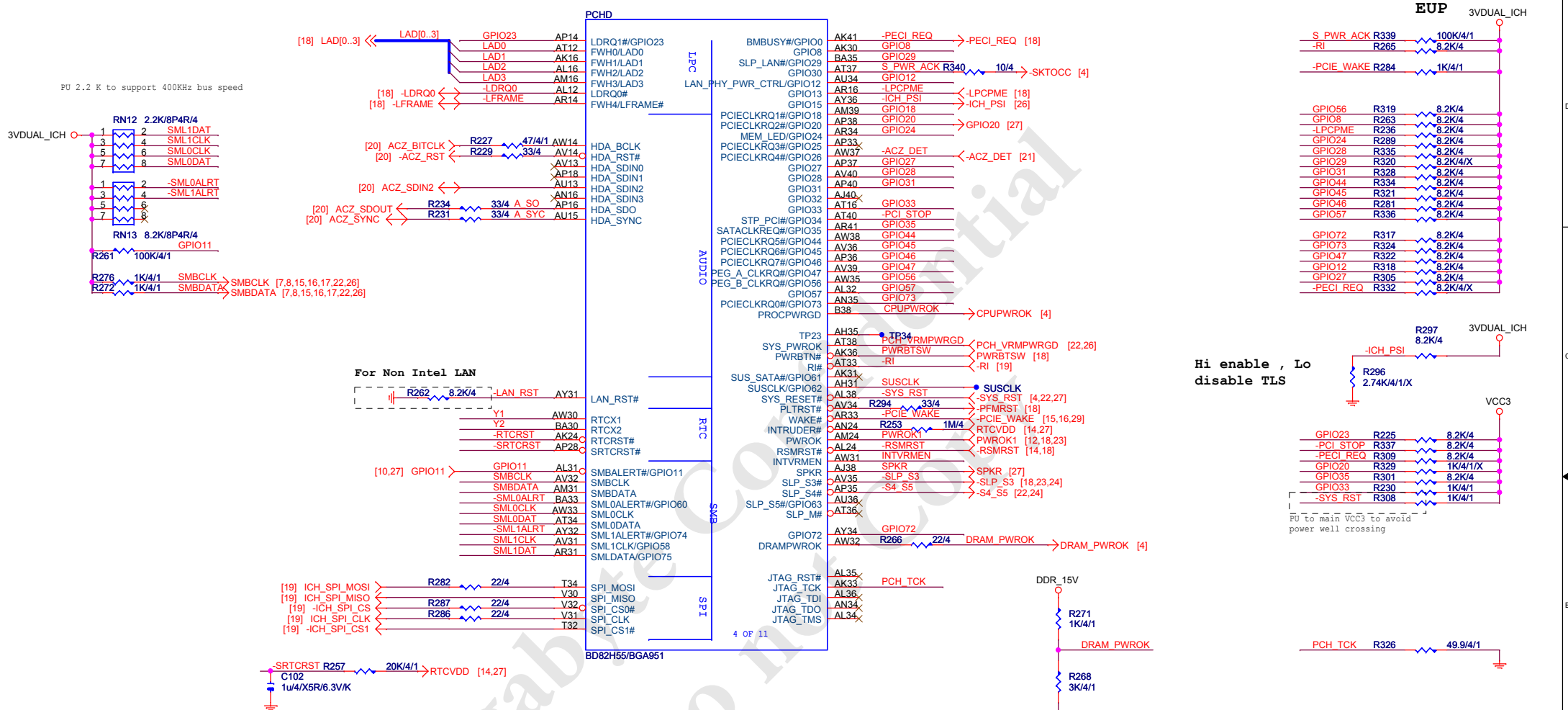
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DDRIII POWER CAP		
Size A	Document Number GA-H55M-S2	Rev 1.3
Date:	Thursday, June 03, 2010	Sheet 9 of 31

DMI:12/5/5/5/12
Impedance=80 +- 17.5%

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%



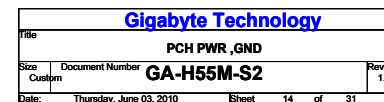


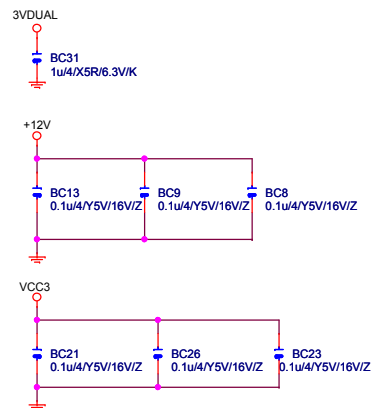
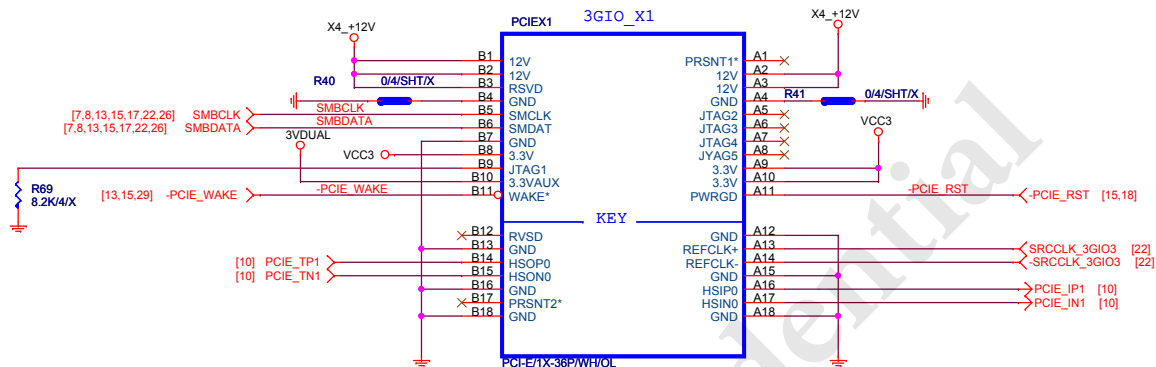
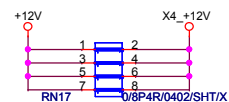


Hi enable , Lo
disable TLS

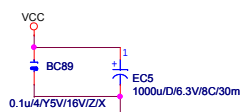
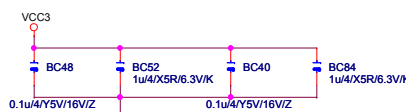
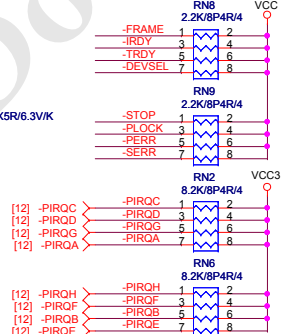
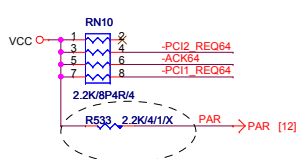
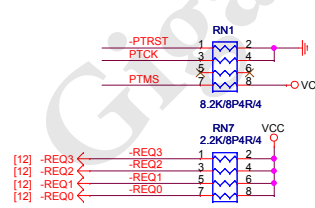
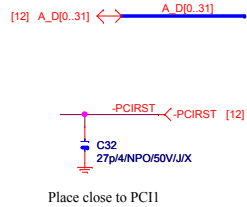
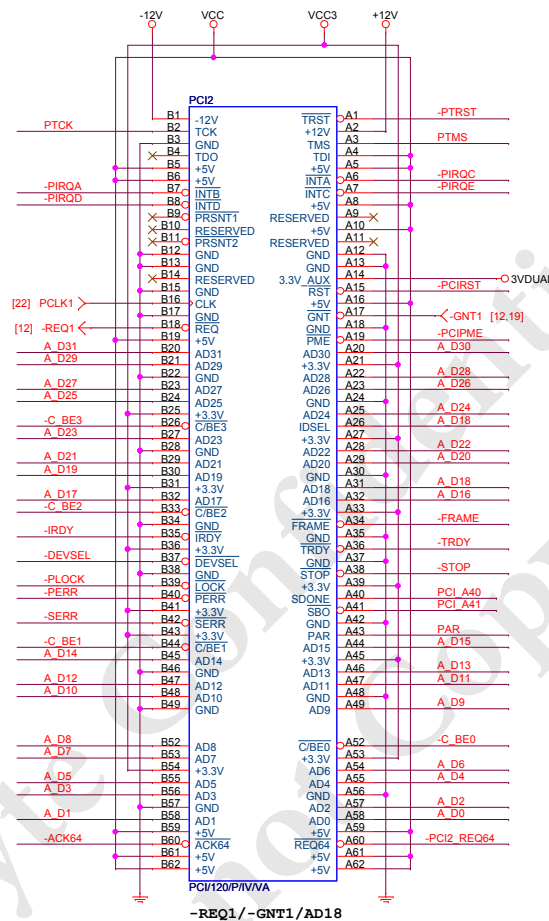
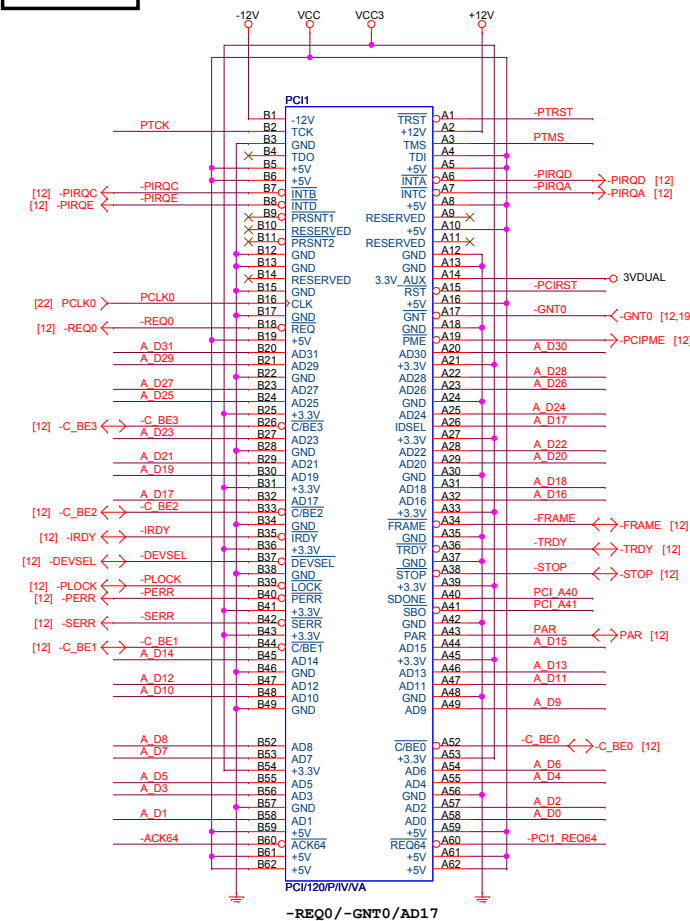
PU to main Vcc3 to avoid
power well crossing

Gigabyte Technology			
PCH GPIO , CTRL , AUDIO			
Title	Document Number	GA-H55M-S2	Rev 1.3
Size B	Thursday, June 03, 2010	Sheet 13 of 31	





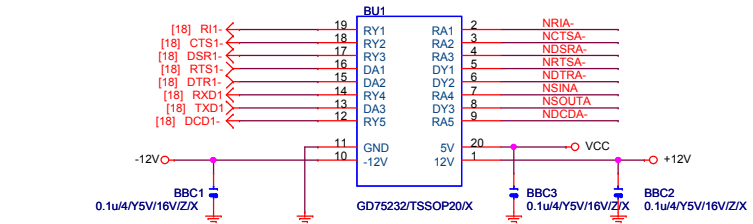
PCI1, 2 SLOT



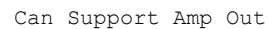
Gigabyte Technology		
PCI SLOT 1, 2		
Title	Document Number	Rev
	GA-H55M-S2	1.3
Size Custom	Date: Thursday, June 03, 2010	Sheet 17 of 31

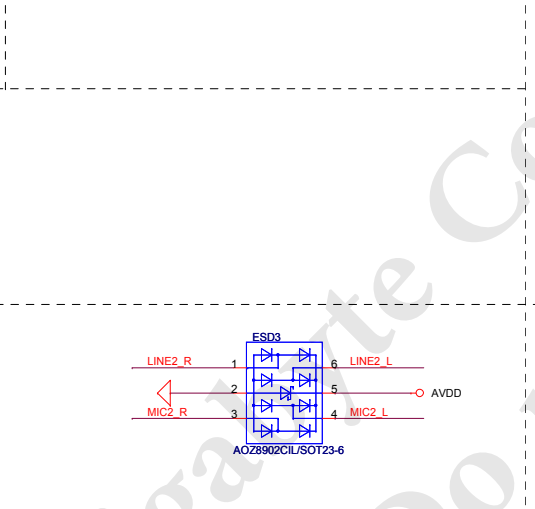
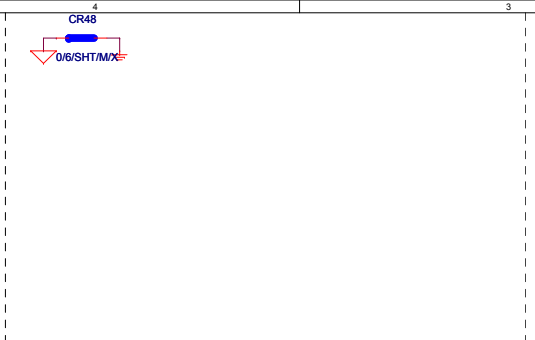
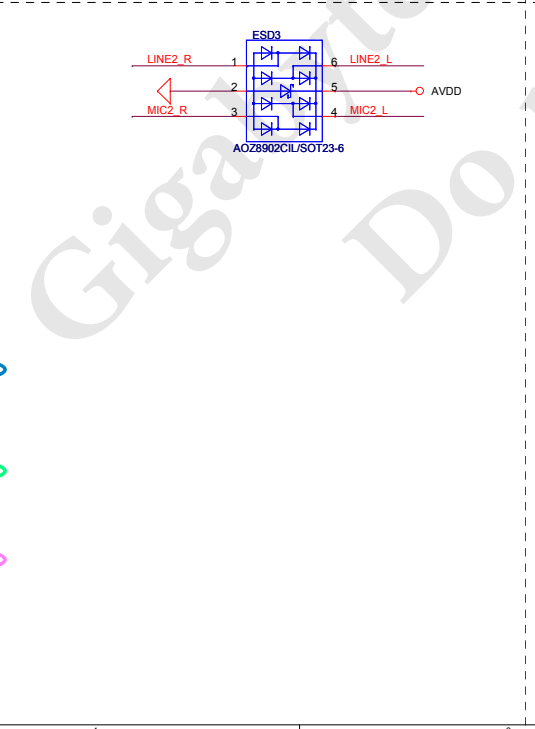
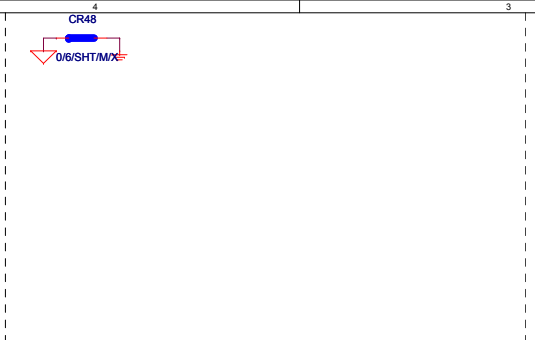
COMB

(N/A)



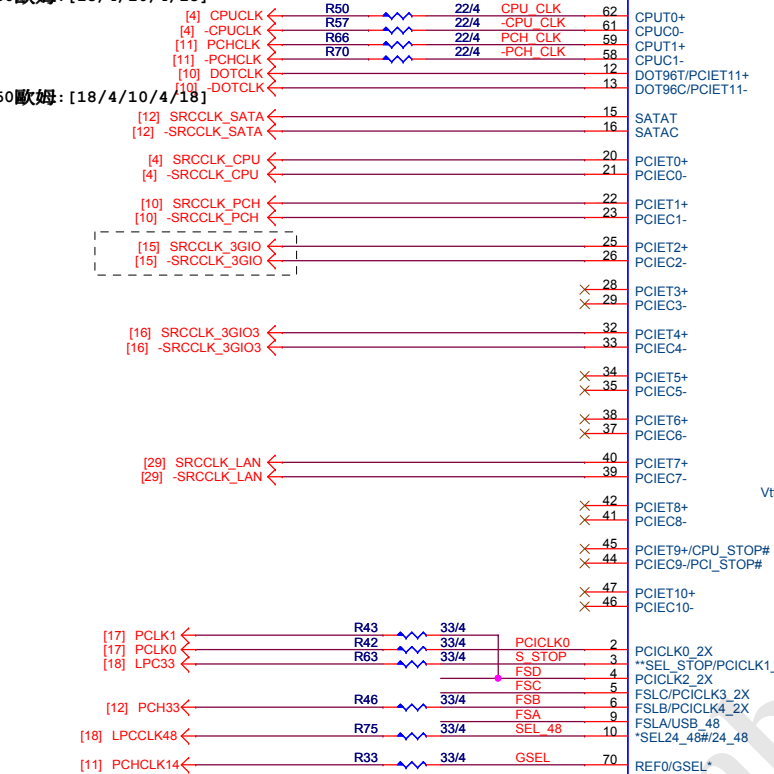
20K/4/0.1% @ALC889A
20K/4/1% @ALC889A+/ALC888Vx



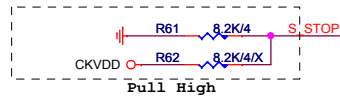
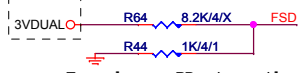


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50歐姆:[18/4/10/4/18]



50歐姆:[4/10]

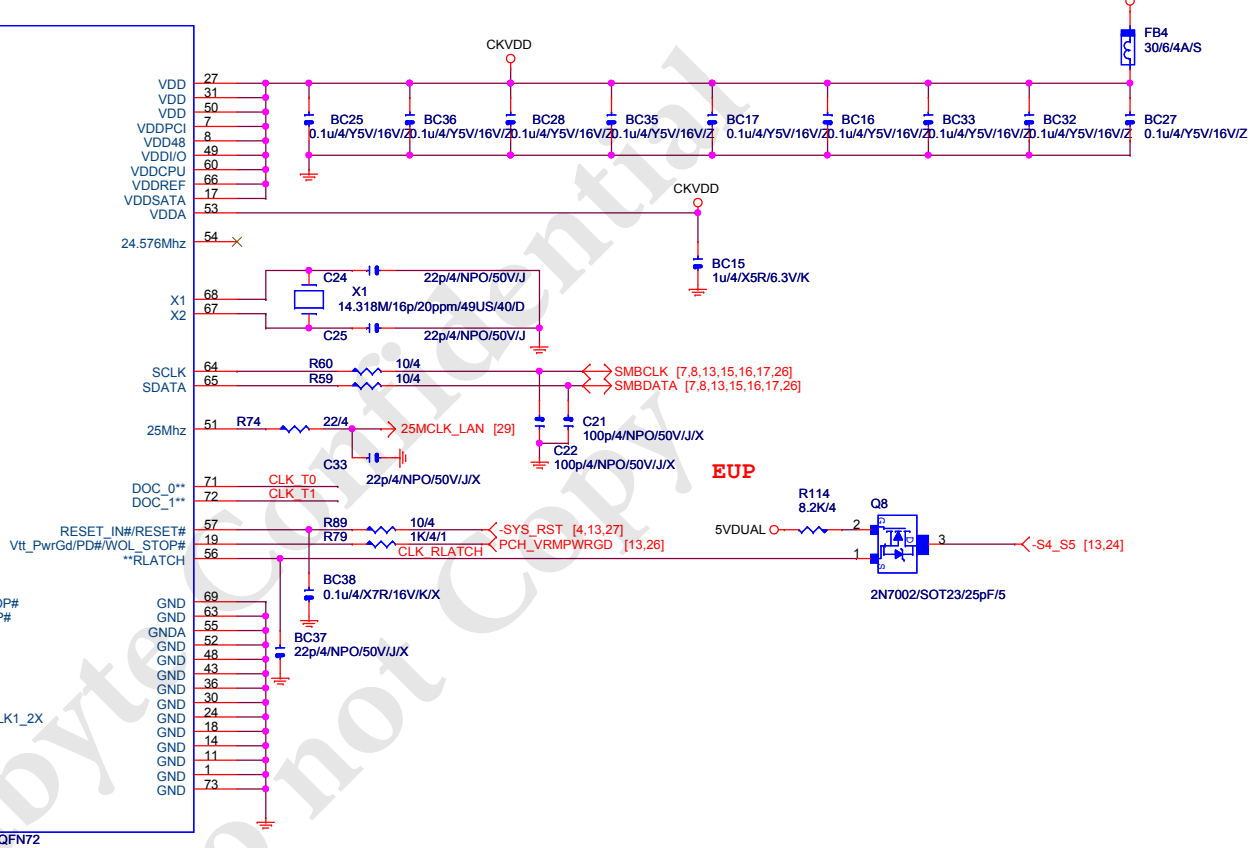


GSEL=1,96Mhz from 12/13
GSEL=0,100Mhz from12/13

SEL_48=1, 24Mhz from pin10
SEL_48=0, 48Mhz from pin10

FSC	FSB	FSA	CPU
0	0	0	266MHz
0	0	1	133MHz
0	1	0	200MHz
0	1	1	166MHz
1	0	0	333MHz
1	1	0	400MHz

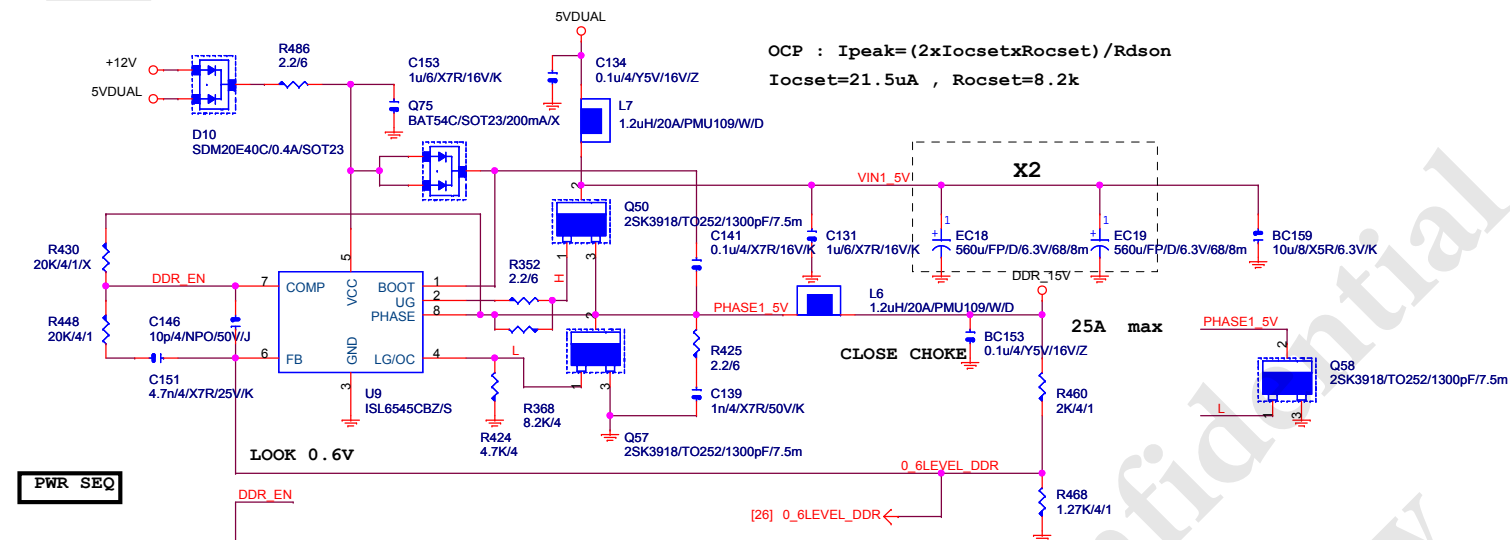
SEL_STOP: latched input to select pin functionality
1 = Selects pin 44/45 to be PCI_STOP#/CPU_STOP#
0 = Selects pin 44/45 to be PCIE outputs ;
3.3V PCICLK output



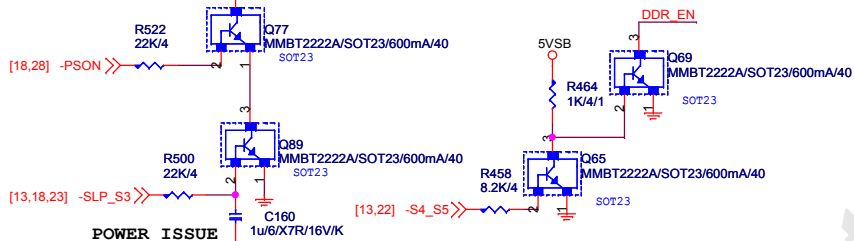
Gigabyte Technology

Title		
CK505 CLK GEN		
GA-H55M-S2		
Size	Document Number	Rev
Custom		1.3
Date:	Thursday, June 03, 2010	Sheet 22 of 31

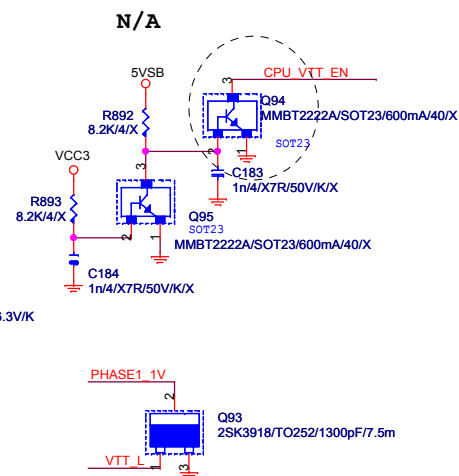
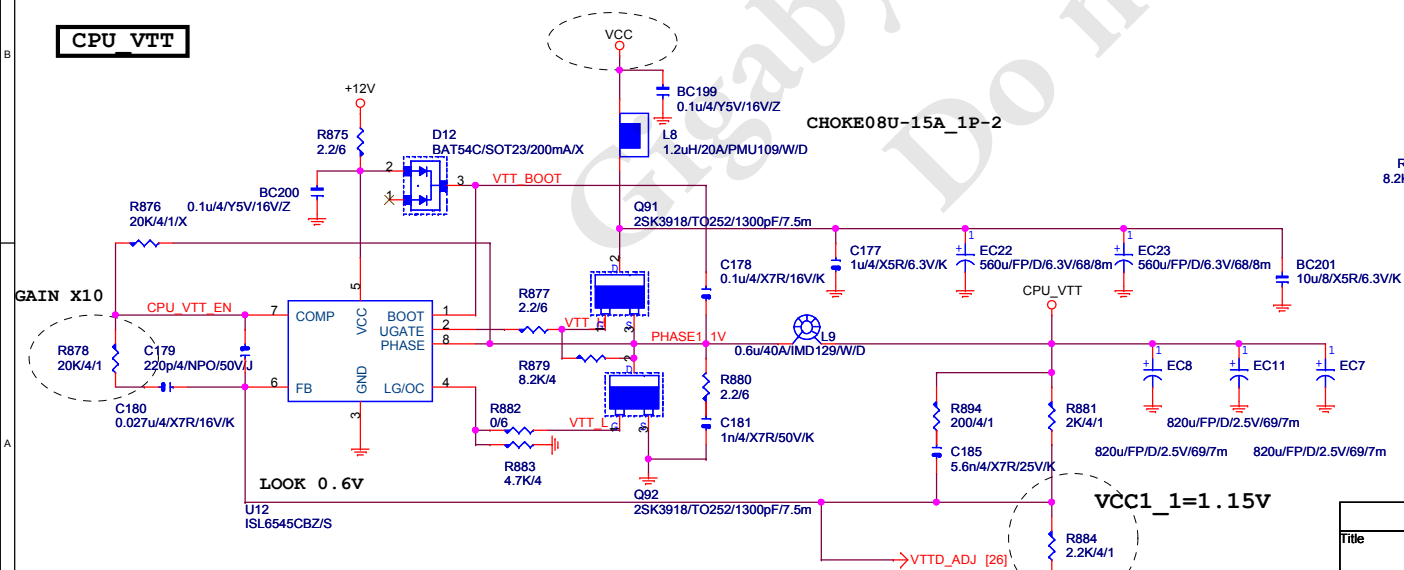
DDR1_5V



PWR	SEQ
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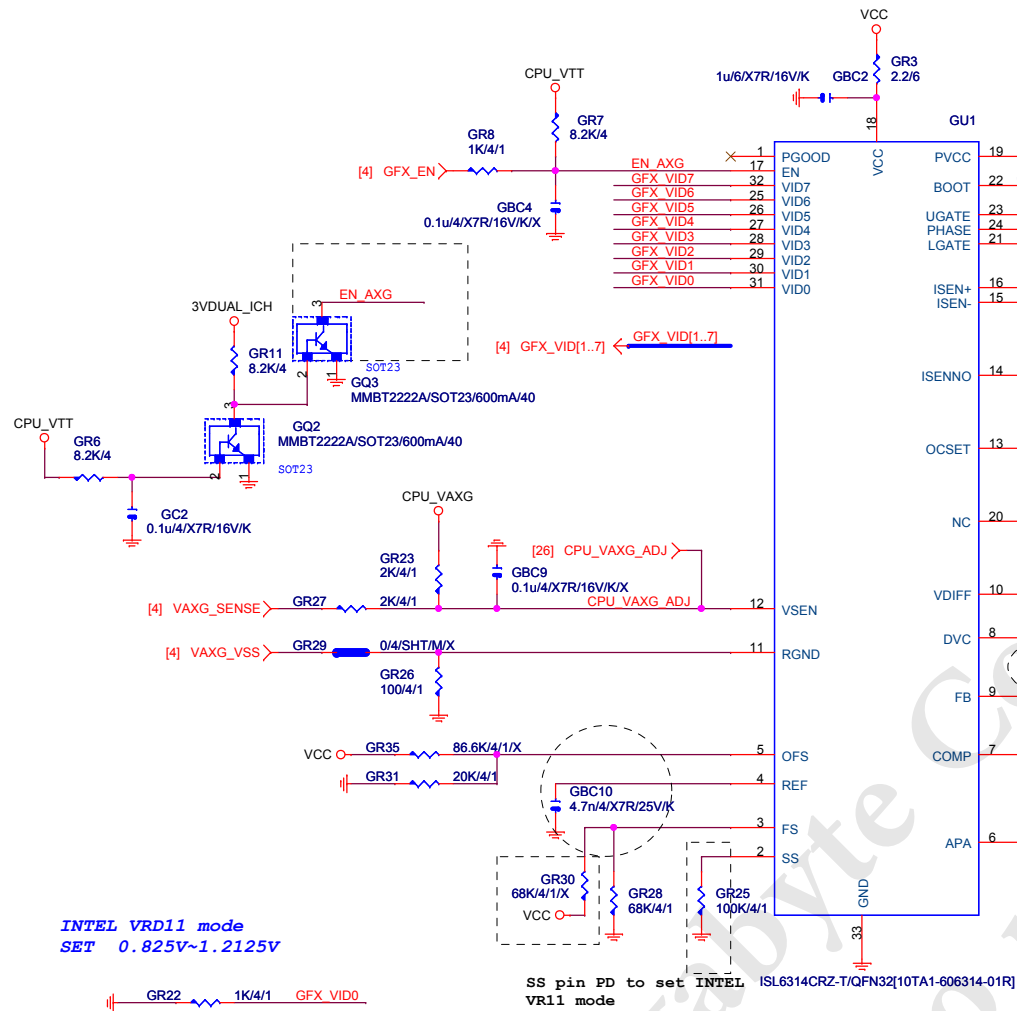
CPU VTT



Gigabyte Technology

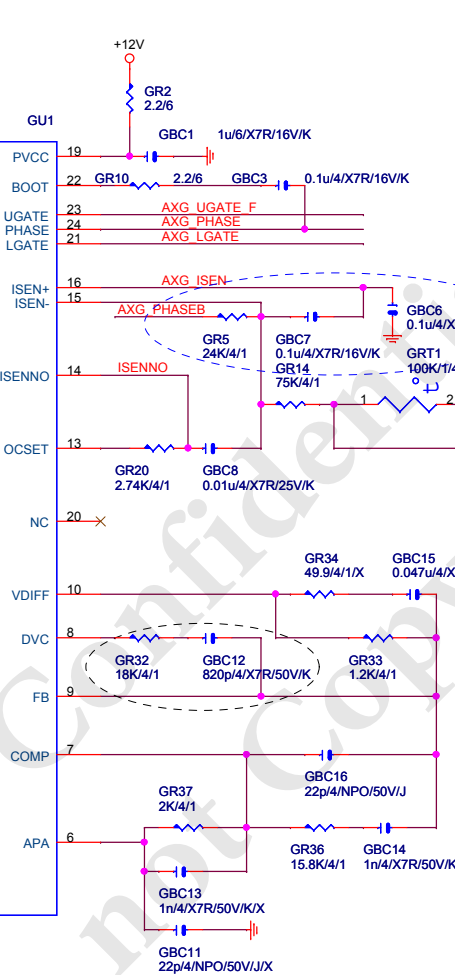
DDR_15Ver **GA-H55M-S2**

Rev	1.3
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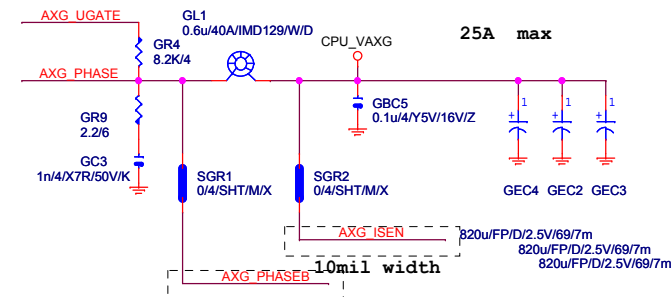


OCP點做在49A
 $R_{ocset}=R_{136}=2.74k$, $I_{sens}=94\mu A$, $R_s=R_{127}=8.25k$,
 $R_{comp}=R_{128}+[R_{135}/((DRT1+R_{129}))]=78k$, $DCR=0.78mohm$
 $I_{ocp}=(R_{ocset}*I_{sens}*R_s)/(R_{comp}*DCR)$
 $=(2.74k*94\mu A*8.25K)/(45K*0.97m)=49A$
 $R_t=10^{[10.61-[1.035X\log(FS)]]}$ $R_t=R_{151}=68\text{ kohm}$, $FS=380KHz$
 $OVP=VDAC+175mV$

PWM IC internal PU

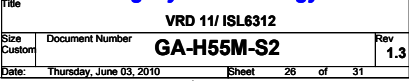


IAXG for 2009A FMB (73W TDP SKU support): 20A
 IAXG for 2009B FMB (87W TDP SKU support): 25A

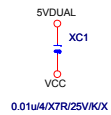
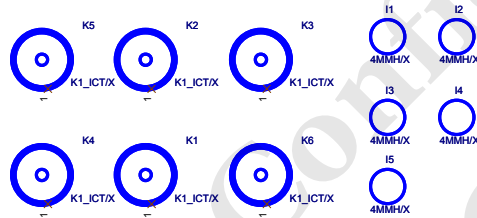
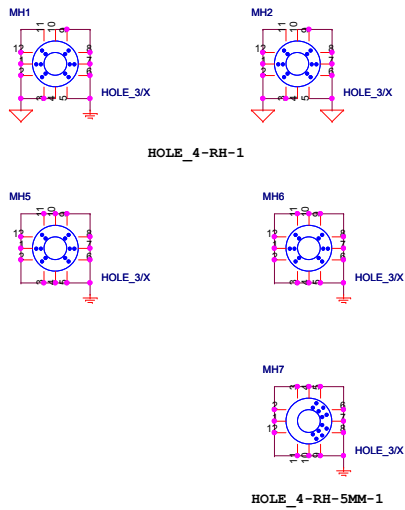
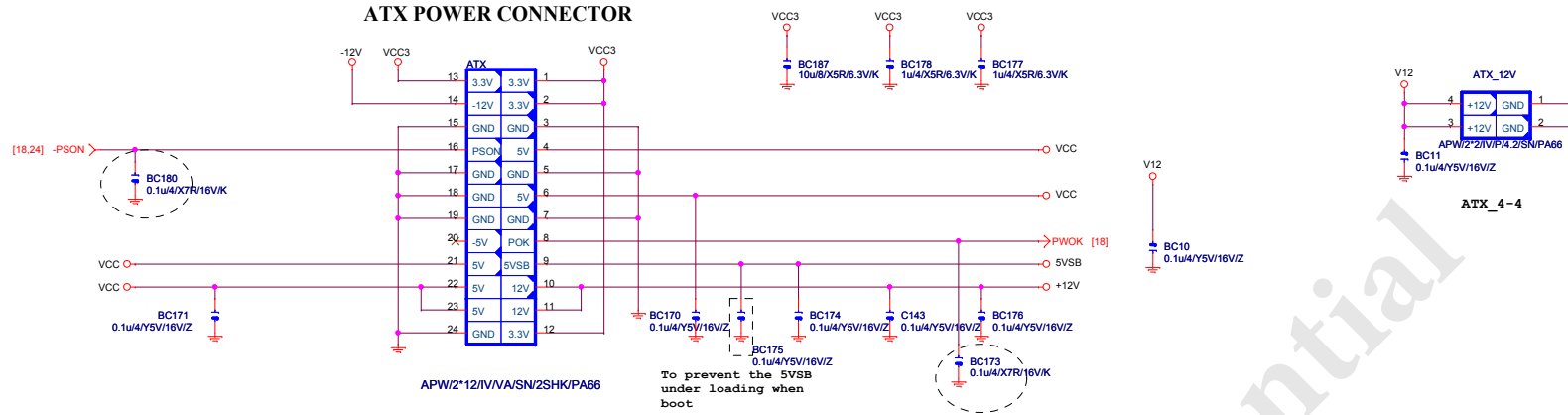


Gigabyte Technology

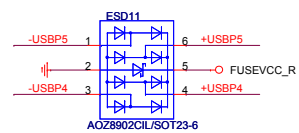
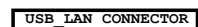
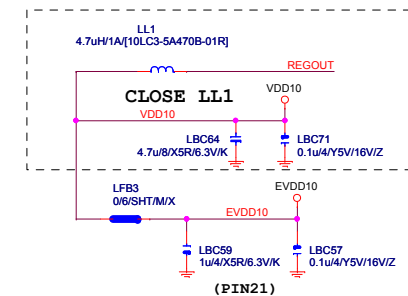
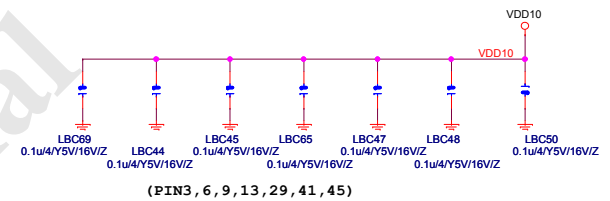
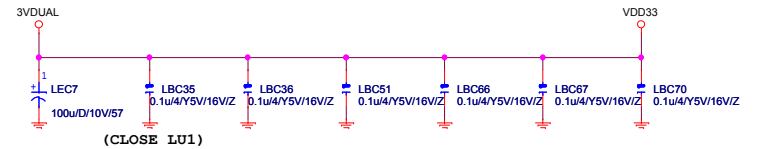
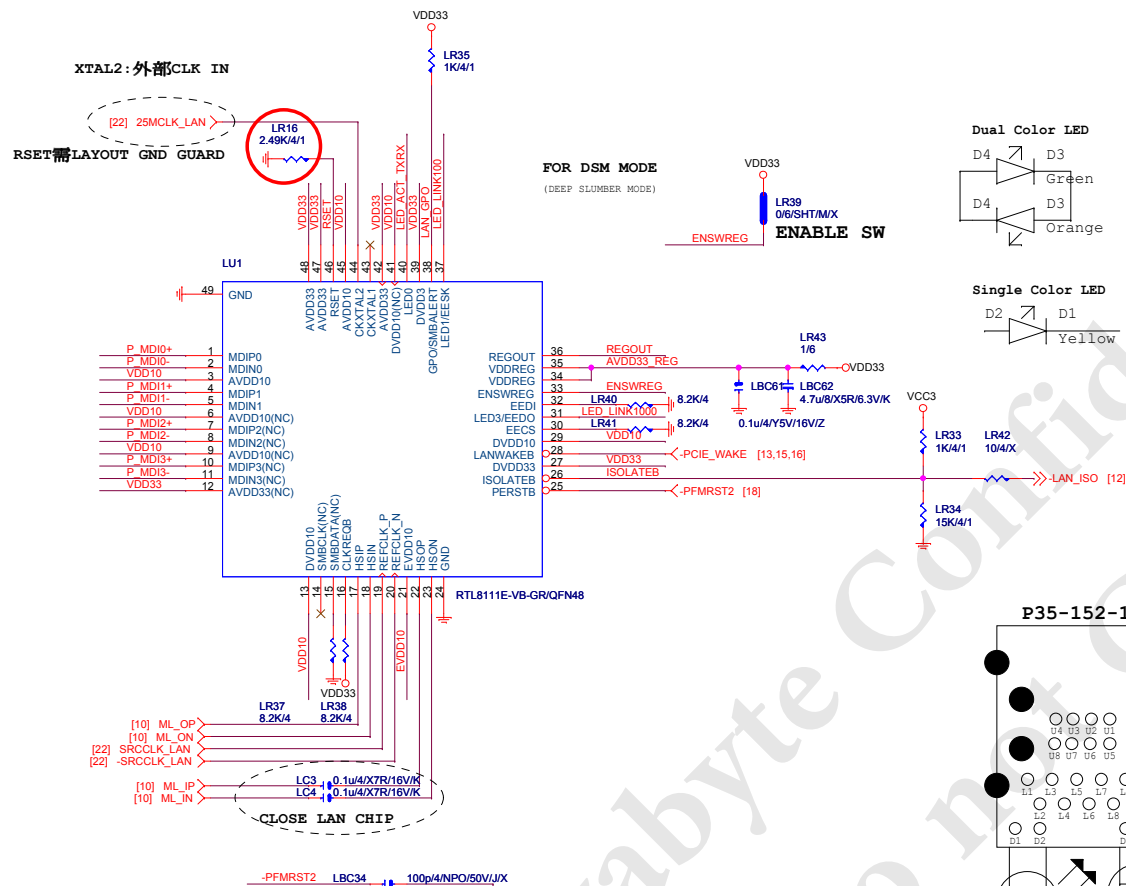
Title		
CPU_VAXG_ISL6314CRZ		
Size	Document Number	Rev
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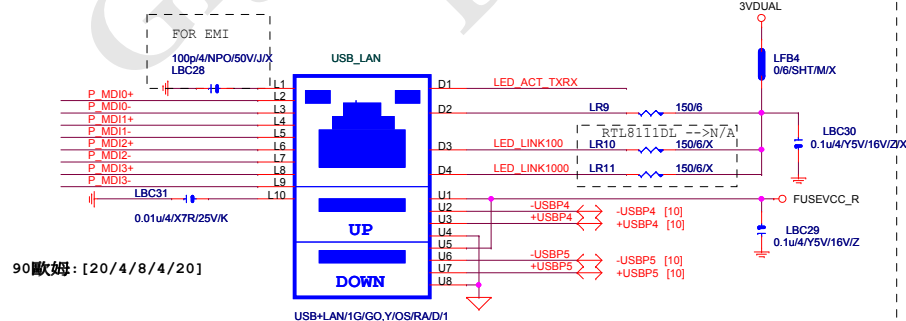
ATX POWER CONNECTOR



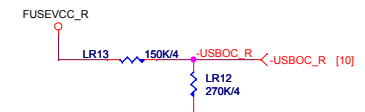
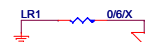
PCIE-1G LAN



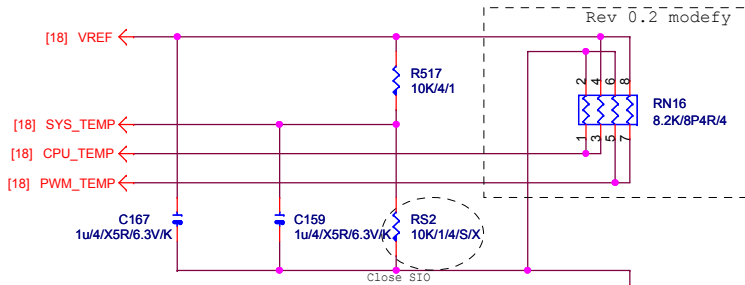
Close to connector



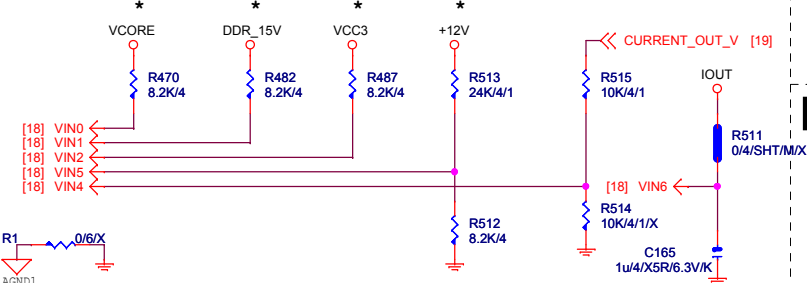
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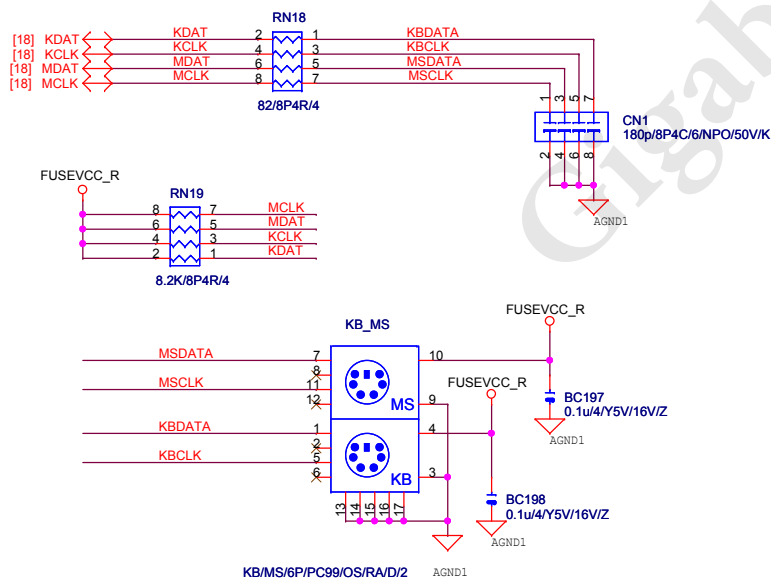
TEMP H/W MONITOR



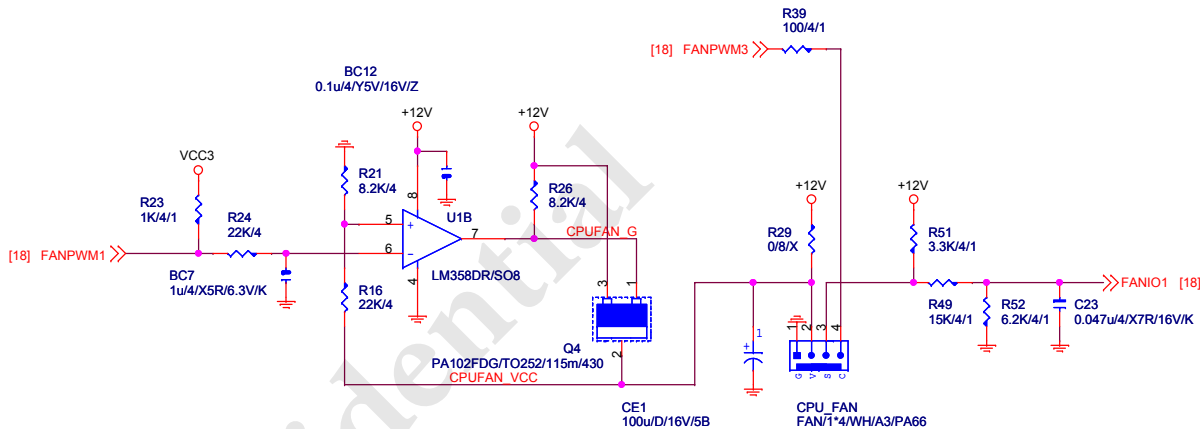
VOLTAGE-- H/W MONITOR



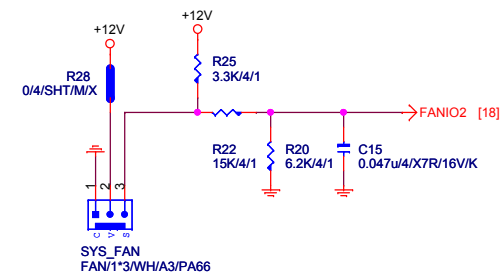
KB/MS



CPU SMART FAN



SYS SMART FAN Linear SYS_FAN



Gigabyte Technology

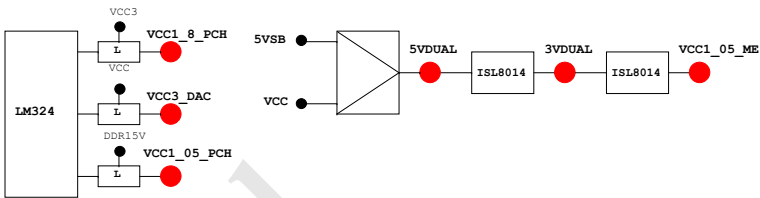
Title				Rev 1.3
HWM,KB/MS, FAN CTRL				
Size	Document Number			
Custom	GA-H55M-S2			
Date:	Thursday, June 03, 2010	Sheet	30 of 31	

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

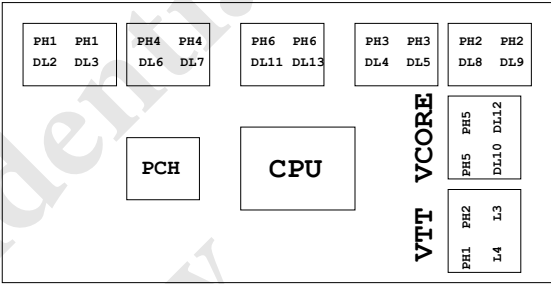
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSIO	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	32 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VIDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號:

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組) 包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH